Docket No.: P-0239 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :
:
Woon Jin JUNG :
:
Serial No. New U.S. Patent Application :
:
Filed: August 31, 2001 :
:
For: JITTER REDUCING APPARATUS USING DIGITAL MODULATION TECHNIQUE

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D. C. 20231

Sir:

Prior to initial examination on the merits, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Please amend the specification by replacing paragraphs as follows:

A. Specification Paragraphs With Mark-ups to Show Changes Made

The following are mark-ups to show changes made to paragraph 27 starting at page 6, and ending at page 7:

[27] ES 1 is a buffer that stores data flowing in from the SDH network, having a size of 8 bytes (width) x 32 (depth). Modulation sequencer 7 generates a mode-value signal and a mode-slope signal representing a modulation frequency having a certain period and amplitude and applies these signals to the phase level detector 2a. The phase level detector 2a compares

an offset (i.e., difference) value of the WAD[4:0] and RAD[4:0] signals of ES 1 to a preset reference value and controls the pattern generator 3 with the digital modulation frequency applied from the modulation sequencer 7. The operation of the phase level detector 2a is described more fully below.

The following are mark-ups to show changes made to paragraph 31 starting at page 7 and ending at page 7:

[31] The WAD[4:0] and RAD[4:0] signals are comprised of five bits and the Mode value[1:0] signal has two bits. The arithmetic operation produces a five bit result having a value [The result value of the operation is] in the range of 0~31. If the result value is between 0 and 15, the phase level detector 2a outputs '0' (H/L Req signal). If the result value is between 16 and 31, the phase level detector 2a outputs '1' (H/L Req signal), to control the pattern generator 3.

After paragraph 31, insert the following new paragraph:

[New] The phase level detector 2a operation has the following effect. If the difference between the WAD[4:0] and RAD[4:0] signals is small, that is if the result of the arithmetic operation is a value between zero and fifteen, then only a small amount of data has been stored in ES 1 and, thus, the output rate of the buffered data should be decreased. On the other hand, if the difference between the WAD[4:0] and RAD[4:0] signals is large, that is if the result of the arithmetic operation is a value between sixteen and thirty-one, then a large amount of data has been stored in ES 1 and the output rate of the data should be increased.

B. Clean Specification Changes

Please replace paragraph 27 starting at page 6, and ending at page 7 with the following:

[27] ES 1 is a buffer that stores data flowing in from the SDH network, having a size of 8 bytes (width) x 32 (depth). Modulation sequencer 7 generates a mode-value signal and a mode-slope signal representing a modulation frequency having a certain period and amplitude and applies these signals to the phase level detector 2a. The phase level detector 2a compares an offset (i.e., difference) value of the WAD[4:0] and RAD[4:0] signals of ES 1 to a preset reference value and controls the pattern generator 3 with the digital modulation frequency applied from the modulation sequencer 7. The operation of the phase level detector 2a is described more fully below.

Please replace paragraph 31 starting at page 7, and ending at page 7 with the following:

[31] The WAD[4:0] and RAD[4:0] signals are comprised of five bits and the Mode_value[1:0] signal has two bits. The arithmetic operation produces a five bit result having a value in the range of 0~31. If the result value is between 0 and 15, the phase level detector 2a outputs '0' (H/L Req signal). If the result value is between 16 and 31, the phase level detector 2a outputs '1' (H/L Req signal), to control the pattern generator 3.

After paragraph 31, insert the following new paragraph:

[New] The phase level detector 2a operation has the following effect. If the difference between the WAD[4:0] and RAD[4:0] signals is small, that is if the result of the arithmetic operation is a value between zero and fifteen, then only a small amount of data has been stored in ES 1 and, thus, the output rate of the buffered data should be decreased. On the other hand, if the difference between the WAD[4:0] and RAD[4:0] signals is large, that is if the result of the arithmetic operation is a value between sixteen and thirty-one, then a large amount of data has been stored in ES 1 and the output rate of the data should be increased.

REMARKS

Claims 1-10 are pending. The specification has been amended to further clarify the invention. Prompt examination and allowance in due course are respectfully solicited.

Respectfully submitted,
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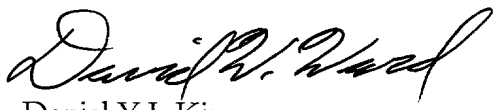

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